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GRAYBEAL, JACKSON, HALEY LLP
155 - 108TH AVENUE NE
SUITE 350
BELLEVUE, WA 98004-5901

EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,382	ZHOU ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28,29,39-44 and 62* is/are allowed.

6)☒ Claim(s) *1-27,30-38,45-61 and 63-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1-3,5,8-17,20, 23-25, 30-31, 33-38, 45- 46, 48-54, 56, 58,59, 63,65-70** are rejected under 35 U.S.C. 102(b) as being anticipated by **Shono**, U.S. Pat. No. **5,436,736**.

Considering claim **1**, Shono discloses all claimed subject matter, note;

a) the claimed a pixel circuit operable to, compare a pixel value to a threshold value, is met by Comparator 23, Fig.4;

b) modify the pixel value...is met by the Adder 22, fig.4; (See col. 5, lines 55-65)

c) the claimed if the pixel value has a predetermined relationship to the threshold value, is inherent, because although the adder does not perform analysis of the conditionality, somewhere in the system a controller, CPU, a microprocessor, or a computer, sets the condition at which the addition, or any other operation, would be performed.

Considering claim **2,** the image processing circuit of claim 1 wherein the pixel value comprises a luminance pixel value, is **inherent** because in each pixel the luminance and color difference components would be represented.

Considering claim **3,** the image processing circuit of claim 1 wherein the pixel value comprises a chrominance pixel value.

See rejection of claim 2.

Considering claim **5**, the image processing circuit of claim 1 wherein the compensation value comprises a randomly generated value, is met by the numbers or values generated by the random number generator 24, fig.4;

Considering claim **8,** the image processing circuit of claim 1 wherein the pixel circuit is operable to modify the pixel value if the pixel value is less than the threshold value.

See rejection of claim 1(b).

Considering claim **9**, the image processing circuit of claim 1 wherein the pixel circuit comprises a processor, is **inherent** in such circuits, because without a processor or a controller the circuit would not work properly.

Considering claim **10**, the image processing circuit of claim 1 wherein the pixel circuit is operable to modify the pixel value by adding a compensation value to the pixel value, is met by the adder which adds the binarized BL signal to the pixel signal fH, fig.4;

Considering claim **11**, an image processing circuit, comprising

a) a pixel circuit operable to generate a random number, is met by Random Number Generator 24, Figs.4 and 6;

b) combine the random number with a pixel value, is met by Operator 26', Fig. 6

Considering claim **12**, wherein the pixel circuit is further operable to truncate the random number before combining the random number with the pixel value, *is inherent because the random number would have to be suitably sized before being combined with the pixel value for successful, desired output.*

Considering claim **13**, the pixel circuit is further operable to clip the pixel value if the pixel value is outside of a predetermined range, is inherent as well *because the pixel value would have to be suitably sized for successful or desired output.*

Considering claim **14**, the image processing circuit of claim 11 wherein the pixel circuit is operable to add the random number to the pixel value, is met by adder 22,Fig.1;

Considering claim **15**, Shono discloses all claimed subject matter, note;

a) a pixel circuit operable to, compare a first pixel value to a first threshold value, the first pixel value corresponding to a pixel location in a first video frame, is met by comparator 23, Fig.4; (see also fig. 6)

b) add a first compensation value to the first pixel value if the first pixel value is

less than the first threshold value, is met by Adder 22, fig.4; (see also rejection of claim 1(c)).

c) compare a second pixel value to a second threshold value, the second pixel value corresponding to the pixel location in a second video frame, add a second compensation value to the second pixel value if the second pixel value is less than the second threshold value, i*s inherent because the system would repeatedly generate random numbers one after the other as needed and repeat the process again and again. (see also fig. 5)*

Considering claim **16**, the image processing circuit of claim 15 wherein the first and second pixel values comprise respective luminance pixel values.

See rejection of claim 2.

Considering claim **17, t**he image processing circuit of claim 15 wherein the first and second 5 pixel values comprises respective chrominance pixel values.

See rejection of claims 2;

Considering claim **20**, the image processing circuit of claim 15 wherein the first and second compensation values comprise respective randomly generated numbers, is met by the random numbers generated by random number generator 24, Fig.4;

Considering claim **23, t**he image processing circuit of claim 15 wherein the pixel circuit is further operable to:

compare the first sum of the first pixel and first compensation values and the second sum of the second pixel and second compensation values to zero; and

set the first pixel value equal to zero if the first sum is less than zero and set the second pixel value equal to zero if the second sum is less than zero.

Considering claim 24, an image processing circuit, comprising

a) a pixel circuit operable to generate a first random number using a first seed number, is met by Random Number Generator 24, Fig.**4;**

b) compare a first pixel values to a first threshold value, is met by the comparator 23, fig.4;

c) add the first random number to the first pixel value if the first pixel value is less than the first threshold value, is met by the Adder 22, fig.4; (see also rejection of claim 1(c) and Fig.6).

d) generate a second random number using a second seed number, compare a second pixel value to a second threshold value, and add the second random number to the second pixel value if the second pixel value is less than the second threshold value, *is*

inherent, because the system would repeatedly generate random numbers one after the other as needed and repeat the process again and again. (see also fig. 5)

Considering claim **25**, wherein the pixel circuit is operable to truncate the first random number before adding the first random number to the first pixel value; and truncate the second random number before adding the second random number to the second pixel value;

Regarding claim 25, see rejection of claim 12.

Considering claim **30**, the image processing circuit of claim 24 wherein:
the first pixel value corresponds to a first pixel location in an image; and
the second pixel value corresponds to a second pixel location in the image,
the second pixel location contiguous with the first pixel location, is **inherent** in a pixel image display system.

Considering claim **31**, an image processing circuit, comprising
a) a pixel circuit operable to, generate a first random number using a first seed number, is met by Random Number Generator 24, Fig.**4;** (see also fig. 6)

b) compare a first pixel value to a first threshold value, the first pixel value corresponding to a starting pixel location in a first video frame, is met by the comparator 23, fig.4; (see also fig. 6)

c) add the first random number to the first pixel value if the first pixel value is less than the first threshold value**,** is met by the Adder 22, fig.4; (see also rejection of claims 1(c) and claim 24 (c)).

d) generate a second random number using a second seed number, compare a second pixel value to a second threshold value, the second pixel value corresponding to a starting pixel location in a second video frame, add the second random number to the second pixel value if the second pixel value is less than the second threshold value, *is inherent because the system would repeatedly generate random numbers one after the other as needed and repeat the process again and again. (see also fig. 5)*

Considering claim **33**, the image processing circuit of claim 31 wherein the pixel circuit is further operable to: a) generate a third random number using a third seed number; b) compare a third pixel value to a third threshold value, the third pixel value corresponding to an ending pixel location in the first video frame; c) add the third random number to the third pixel value if the third pixel value is less than the third threshold value; and d) set the second seed number equal to the third random number.

See rejection of claim 31 (d).

Considering claim **34**, the image processing circuit, wherein the pixel circuit is operable to: generate a first random number, add the first random number to a first pixel value,

generate a second random number, and add the second random number to a second pixel value.

Regarding claim 34, see rejection of claims 1, 24, and 31; (see also fig. 6)

Considering claim **35**, the image processing circuit of claim 34 wherein the pixel circuit is operable to generate the first and second random numbers from respective first and second seed numbers, is met by the Random number generator 24; (see also col. 5, lines 55-65)

Considering claim **36**, the image processing circuit of claim 34 wherein the pixel circuit is operable to: generate the first random number from a seed number; and generate the second random number from the first random number.

See rejection of claim 34;

Considering claim **37**, the image processing circuit of claim 34 wherein:
the first pixel value corresponds to a pixel location in a first video frame; the second pixel value corresponds to the pixel location in a second video frame; and the first random number equals the second random number.

See rejection of claim 30;

Considering claim **38,** the image processing circuit of claim 34 wherein: the first pixel value corresponds to a starting pixel location in a first video frame; the second pixel

value corresponds to the pixel location in a second video frame; and the first random number does not equal the second random number, is inherent in a pixel image display system. (see rejection of claim 30)

Claim **45**, is a method claim of claim 1 and thus, claim 45 is rejected for the same reasons as claim 1;

Considering claim **46**, the method of claim 45, further comprising: generating a random number; setting the compensation value equal to the random number.

See rejection of claim 7;

Considering claim **48**, the method of claim 45, further comprising: determining whether the sum of the pixel and compensation values is within a predetermined range of pixel values; and setting the pixel value equal to a value within the range if the sum is outside of the range.

See rejection of claim 7;

Considering claim **49**, the method of claim 45 wherein the modifying comprises modifying the pixel value if the pixel value is less than the threshold value.

See rejection of claim 8;

Considering claim **50**, the method of claim 45 wherein the modifying comprises adding a

compensation value to the pixel value, is met by Adder 22, fig.4;

Considering claim **51**, a method, comprising:

a) generating a random number, is met by random number generator 24, fig.4;

b) combining the random number with a pixel value, is met by the adder 22, fig.4; (see also fig. 6)

Considering claim **52**, the method of claim 51, further comprising *truncating the random number before combining the random number with the pixel value, is inherent because the random number would have to be suitably sized before being combined with the pixel value for successful, desired output.*

Considering claim **53**, the method of claim 51, further comprising clipping the pixel value if the pixel value is outside of a predetermined range.

See rejection of claim 52;

Claim **54** is a method claim of claim **15** and thus, claim **54** is rejected for the same reasons as claim **15**;

Considering claim **56**, wherein the first and second compensation values equal the same randomly generated number, is met by random number generated by generator 24, fig.4;

Considering claim **58**, see rejection of claim 24;

Considering claim **59**, the method of claim 58 wherein:

the generating the first random number comprises truncating the first random number; and the generating the second random number comprises truncating the second random number, *is inherent because the random number would have to suitably sized before being combined with the pixel value for successful, desired output.*

Considering claim **63**, a method, comprising:

a) generating a first random number using a first seed number;

b) comparing a first pixel value to a first threshold value, the first pixel value corresponding to a starting pixel location in a first video frame;

c) adding the first random number to the first pixel value if the first pixel value is less than the first threshold value;

d) generating a second random number using a second seed number;

e) comparing a second pixel value to a second threshold value, the second pixel value corresponding to a starting pixel location in a second video frame;

f) adding the second random number to the second pixel value if the second pixel value is less than the second threshold value.

See rejection of claims 15 and 24; (see fig. 6)

Considering claim **65,** see rejection of claim **33.**

Considering claim **66**, a method, comprising:

a) generating a first random number,

b) adding the first random number to a first pixel value;

c) generating a second random number;

d) adding the second random number to a second pixel value.

See rejection of claims 15 and 24; (see fig. 6)

Considering claim **67**, the method of claim 66 wherein the generating the first and second random numbers comprises generating the first and second random numbers from respective first and second seed numbers, is inherent because the random number would have some predetermined or programmed way of generating the random numbers.

Considering claim **68**, the method of claim 66 wherein: the generating the first random number comprises generating the first random number from a seed number; and the generating the second random number comprises generating the second random number from the first random number.

See rejection of claim 67;

Considering claim **69**, the method of claim 66 wherein: the first pixel value corresponds to a pixel location in a first video frame; the second pixel value corresponds to the pixel location in a second video frame; the generating the second random number comprises generating the second random equal to the first random number.

See rejection of claim 37;

Considering claim **70**, the method of claim 66 wherein: the first pixel value corresponds to a starting pixel location in a first video frame; the second pixel value corresponds to the pixel location in a second video frame; and the generating the second random number comprises generating the second random number unequal to the first random number.

See rejection of claim 37;

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims **4, 6, 7,18, 19, 21, 22, 26, 27, 32, 55, 60-61, and 64** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shono.

Considering claim **4**, the image processing circuit of claim 1 wherein the threshold value is within a range of approximately 50 - 80.

Regarding claim 4, Shono does not specifically disclose threshold value to be within a range of approximately 50-80. However, it would have been an obvious matter of design choice to modify the Shono reference by having desired range of threshold values, since applicant has not disclosed that having a particular range of 50-80 solves any stated problem.

Considering claim **6**, the image processing circuit of claim 1 wherein the compensation value comprises a randomly generated value within a range of -3 - 3.

Regarding claim 6, see rejection of claim 4;

Considering claim **7**, the image processing circuit of claim 1 wherein the pixel circuit is further operable to: determine whether the sum of the pixel and compensation values is within a predetermined range of pixel values; and set the pixel value equal to a value within the range if the sum is outside of the range.

See rejection of claim 4;

Considering claim **18**. The image processing circuit of claim 15 wherein the first and second threshold values are within a range of approximately 50 - 80.

See rejection of claim 4;

Considering claim **19, t**he image processing circuit of claim 15 wherein the first threshold value equals the second threshold value.

Regarding claim 19, Shono does not specifically disclose the first threshold value equals the second threshold value. However, it would have been an obvious matter of design choice to modify the Shono reference by having first threshold value equals the second threshold value, since applicant has not disclosed that having such equal values solves any stated problem.

Considering claim **21, t**he image processing circuit of claim 15 wherein the first compensation value equals the second compensation value.

See rejection of claim **4**;

Considering claim **22**. The image processing circuit of claim 15 wherein the first and second compensation values comprise respective randomly generated numbers within a range of -3 – 3;

See rejection of claim 4;

Considering claim **26**, the image processing circuit of claim 24 wherein the second seed number equals the first random number.

Shono does not specifically disclose whether the second seed number equals the first random number. However, it would have been an obvious matter of design choice to modify the Shono reference by having the second seed number equals the

first random number, since applicant has not disclosed that particularly having the second seed number equaling the first random number solves any stated problem.

Considering claim **27**, the image processing circuit of claim 24 wherein the second seed number equals the first seed number.

See rejection of claim 26.

Considering claim **32**, the image processing circuit of claim 31 wherein the second seed number equals the first seed number.

See rejection of claim 26.

Considering claim **55**, the method of claim 54 wherein the first threshold value equals the second threshold value.

See rejection of claim 19.

Considering claim **60**, the method of claim 58 wherein the second seed number equals the first random number.

See rejection of claim 19.

Considering claim **61**, the method of claim 58 wherein the second seed number equals the first seed number.

See rejection of claim 19.

Considering claim **64**, comprising setting the second seed number equal to the first seed number.

See rejection of claim 19.

Response to Arguments

5. Applicant's arguments filed Feb. 24, 2004 have been fully considered but they are not persuasive. Response follows.

Applicnat's arguments

a) Regarding claims 1 and 45: However, Shono fails to teach that the adder 22 in any way qualifiedly adds the data. That is, the binaries data is combined with the higher-order bit data(i.e. modified) irrespective of any precondition (e.g. a threshold value relationship, as claimed.

b) Shono, on the other hand, fails to teach or suggest a random number and pixel value being combined or added to one another.

Examiner's response

a) Regarding claims 1 and 45, an adder is an adder, is an adder. There is not analysis of input data performed in the claimed adder either. The claimed adder 106 simply adds. Somewhere in the system, a controller, a CPU or a similar logic controls the

conditionality of the process. Therefore, that the adder of Shono is not "qualifiedly" adding the data input to it, while, at the same time, the claimed adder 106 does so, impliedly at least, is unpersuasive.

b) See figure 6, which combines the output of random number generator and fH output from the operator 25. See also col. 5, lines 56-59 wherein is specifically taught that pixel data is input to the operator 25 where the pixel data is divided into fH and fL, higher and lower-order bit data, respectively, which nonetheless is still pixel data. Thus, the argument that Shono fails to teach or suggest a random number and pixel value being combined or added to one another, is unpersuasive.

Allowable Subject Matter

6. Claims **28,29 and 39-44** are allowable over the prior art.

7. Claim **62** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose image processing circuit, wherein the pixel circuit is operable to: *truncate* the first random number before adding the first random number to the first pixel value; *truncate* the second random number before adding the second random number to the second pixel value; set the second seed number equal to the *untruncated* first random number, as in claim **28**; wherein generating the first and

second random numbers comprises generating the first and second random numbers according to the following equation: random number= (1664525 x seed number+ 1013904223)mod 232, as in claims **29** and **62**, and a comparator having a pixel value input terminal and a first and second pixel value output terminals, as in claim 39.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PAULOS M. NATNAEL
PATENT EXAMINER

PMN
May 15, 2004